3. The high-voltage transistor according to claim **1** wherein each of the drift regions has a width in the first lateral direction that is substantially equal.

4. The high-voltage transistor according to claim **1** wherein the width of the inner and outer regions is substantially the same at all points in the first and second lateral directions.

5. The high-voltage transistor according to claim **1** wherein the substrate comprises a planar bottom surface, the vertical direction being oriented perpendicular to the planar bottom surface and the lateral direction being oriented parallel to the planar bottom surface.

6. The high-voltage transistor according to claim **1** wherein each of the drift regions have a length oriented in the vertical direction and a width oriented in the first lateral direction, the length being more than five times the width.

7. The high-voltage transistor according to claim **1** wherein the first conductivity type comprises n-type.

8. The high-voltage transistor according to claim **1** wherein the field plate member extends in the vertical direction, oriented substantially parallel to the drift regions.

9. A high-voltage transistor comprising:

a substrate having a top surface;

a drain of a first conductivity type;

a source of the first conductivity type;

a body region of a second conductivity type opposite to the first conductivity type, the body region adjoining the source region, a conductive channel being formed in the body region when the high-voltage transistor is in an on-state such that current flows between the source and drain;

a drift region of the first conductivity type extending in a vertical direction from the drain to the body region;

a field plate member that laterally encircles the drift region, the field plate member being disposed in a dielectric layer, the field plate member having an entire length that extends in the vertical direction from a beginning at the top surface of the substrate downward to a farthest end of the field plate member, an inner region of the dielectric layer laterally separating the drift region from the field plate member and an outer region of the dielectric layer laterally separating the field plate member from a perimeter semiconductor region of the substrate that extends in the vertical direction downward from the top surface, the inner and outer regions each having a width that is substantially the same at all points along the entire length of the field plate member; and

an insulated gate disposed in the inner region of the dielectric layer adjacent the body region, application of a voltage potential to the insulated gate causing the conduction channel to form in the body region.

10. The high-voltage transistor according to claim **9** wherein the drift region extends in a lateral direction, terminating at each end in a rounded fingertip area.

11. The high-voltage transistor according to claim **10** wherein the substrate comprises a planar bottom surface, the vertical direction being oriented perpendicular to the planar bottom surface and the lateral direction being oriented parallel to the planar bottom surface.

12. The high-voltage transistor according to claim **9** wherein the perimeter semiconductor region extends from the top surface to a drain electrode formed on a bottom surface of the substrate.

13. The high-voltage transistor according to claim **9** wherein the perimeter semiconductor region is laterally separated from the field plate member by a distance that is substantially the same at all points along an outer edge of the field plate member.

14. The high-voltage transistor according to claim **9** wherein the drift region has a length oriented in the vertical direction and a width oriented in a first lateral direction, the length being more than five times the width.

15. A power transistor comprising:

a substrate having a top surface, an active device area, and a perimeter area of a first conductivity type, the active device area including:

a drain region of the first conductivity type;

a plurality of source regions of the first conductivity type, each source region being disposed at or near the top surface of the substrate;

a plurality of body regions of a second conductivity type, each body region being disposed beneath a corresponding one of the source regions; and

a plurality of drift regions of the first conductivity type extending in a vertical direction from a corresponding one of the body regions downward to the drain region, adjacent ones of the drift regions being separated in a first lateral direction by a dielectric layer, each of the drift regions terminating in a second lateral direction in a fingertip area;

a field plate member disposed within the dielectric layer that surrounds each of the drift regions in the first and second lateral directions, the field plate member having an entire length that extends in the vertical direction from a beginning at the top surface of the substrate downward to a farthest end of the field plate member, an inner region of the dielectric layer laterally separating the drift regions from the field plate member and an outer region of the dielectric layer laterally separating the field plate member from the perimeter area of the substrate, the inner and outer regions each having a width that is substantially the same at all points along the entire length of the field plate member, the perimeter area being laterally separated from the field plate member by a distance that is substantially the same at all points along an outer edge of the field plate member;

a gate disposed in the dielectric layer between a corresponding one of the body regions and the field plate member, application of a voltage potential to the gate causing a vertical conduction channel to form in the body region such that current flows between the source regions and the drain when the high-voltage transistor is in an on-state.

16. The power transistor of claim **15** wherein the perimeter area extends from the top surface to a drain electrode formed on a bottom surface of the substrate.

17. The power transistor of claim **15** wherein the substrate comprises a planar bottom surface, the vertical direction being oriented perpendicular to the planar bottom surface and the lateral direction being oriented parallel to the planar bottom surface.

18. The power transistor of claim **15** wherein the drift region has a length oriented in the vertical direction and a width oriented in a first lateral direction, the length being more than five times the width.

19. The power transistor of claim **15** wherein the perimeter area comprises a semiconductor region of the first conductivity type.

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